PRN:		Course Code :	U01ES004

First Year **B. Tech** End Semester Examination Winter 2024 000079

Basic Electrical and Electronics Engineering

Day and Date: Fri 6 DEC 2024 Max Marks: **50**

Time : 02:00PM To 04:00PM Duration: **02** hrs

Instructions: All questions are compulsory.

		Marks	Bloom's Level	CO
Q.1	**Solve any five from following**			
a)	State Kirchhoff's current and voltage Laws	2	1	2
b)	Define following terms with units **A.** Resistance **B.** Ohms Law	2	1	1
c)	Define following terms with units and equations **A.** Electric Energy **B.** Electric power	2	1	1
d)	Define following terms with units **A.** Magnetic Flux **B.** Magnetic Flux Density	2	1	1
e)	Draw Energy Band Gap Diagram for **A.** Conductors **B.** Semiconductor	2	1	3
f)	Draw truth table and write equation of following gates **A.** OR Gate **B.** NAND Gate	2	1	4
e)	Write a list of four parameters that can be measured using a Digital Multimeter.	2	1	5
Q.2	**Solve any two from following**			
a)	Calculate the equivalent resistance across battery and current supplied by battery for circuit given below	5	3	2
b)	State and Explain series and parallel circuits with an example	5	1	2
c)	State and explain Kirchhoff's Current Law with an example	5	1	3
Q.3	**Solve any two from following**			
a)	Draw and Explain operation of Common Emitter (CE) configuration of Transistor	5	4	3
b)	Draw and Explain PN Junction diode	5	4	3
c)	Write comparison between P-type and N-type Extrinsic Semiconductor (at least 5 points)	5	2	3

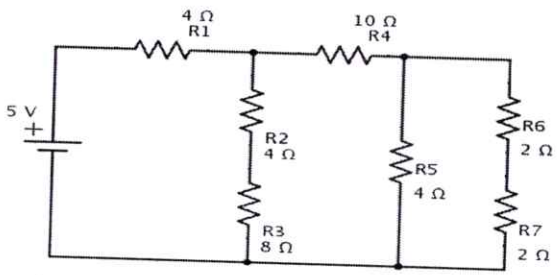


Fig.1.a

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Q.4	**Solve any two from following**				
a)	Describe NOT , XNOR & X-OR gates with truth table	**5**	4	4
b)	Convert the following I. decimal number 155.33 into binary II. Octal $(246.28)_8$ into its decimal III. $(01011111011.011111)_2$ to hexadecimal	**5**	5	4
c)	Design basic AND gate using universal NAND gate and NOR gate	**5**	4	4
Q.5	**Solve any two from following**			
a)	Draw and Explain Block diagram of digital Multimeter	**5**	4	5
b)	Draw and Explain Block diagram of CRO	**5**	4	5
c)	Draw and Explain Block diagram of Signal Generator	**5**	4	5

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